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Datasheet: SD Memory Card Controller AK2705EN

Version 01.03

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1. Foreword

This document has been produced by ASolid Technology Co., Ltd., should the company modifies the contents of this specification, it will be re-released with an identifying change of release date and an increase in revision number as follows:

Revision mn.xy, where:

- mn the first two digit are incremented for major changes of substance, e.g., functional changes.
- xy the second two digits are incremented when minor changes have been incorporated into the specification, i.e., enhancements, corrections, updates, etc.

2. Revision History

Revision	Date	Modified By	Description
01.00	2019/11/28	Document Control Center	Initial version of Datasheet of SD Memory Card Controller AK2705EN
01.01	2019/12/11	Document Control Center	Modify AK2705EN description
01.02	2019/12/17	Document Control Center	Modify AK2705EN package description
01.03	2020/8/24	Document Control Center	Modify AK2705EN description

3. Statement of Scope

This Datasheet document is description the SD Memory Card Controller methods and abstractions of reliability. The contents include the concept and measurement methodologies.

4. General Description

SD Memory Card Controller AK2705EN is the SD controller launched by ASolid Technology Co., Ltd., which utilizes UMC process technology. AK2705EN is featured with higher performance and lower power consumption, and supports SD1.01, SD1.10, SD2.02, SD3.01, SD4.1, SD5.1, SD6.0 and SD6.1. The product is built in with single channel high speed flash interface with advanced error correction code (ECC), and supports all kinds of 3D NAND type flash including TLC and QLC.

4.1. Feature

- Compatible with SD Card standard specification v1.01/v1.1/v2.02/v3.01/v4.1/v5.1/v6.0/v6.1.
  - Supports SPI mode.
  - Supports Bus Speed Mode: Default Speed mode, High Speed mode, SDR12, SDR25, SDR50, SDR104 and DDR50.
  - Copyright Protection Mechanism-Complies with highest security of SDMI standard.
  - Supports standard capacity SD memory card (<= 2GB).
  - Supports SDHC capacity (4GB to 32GB).
  - Supports SDXC capacity (32GB to 2TB).
  - Supports SD command class 0, 2, 4, 5, 6, 7, 8 and 10.
  - Supports password protection and built-in write protection features.
  - Supports CMD queue function
  - Supports Cache function.
  - Supports Function Extension.
  - Supports LVS(Low Voltage Signaling interface)
  - Supports A1,A2(Application performance class)
- SD card interface with programmable output drive capability
- Flash interface support:
  - UP to 1 flash chip selection and 8-bit flash IO access
  - Supports both 1.2V and 1.8V flash IO voltage for SD card
  - Supports both 2.5V and 3.3V flash core voltage for SD card
- Flash memory support:
  - Supports ECC function to correct up to equivalent 16x-bits data errors per 1K bytes data

automatically

- Supports 3D TLC/QLC type NAND flash
- Supports flash with 8KB/16KB page architecture
- Supports four-plane 16KB-page/eight-plane 8KB-page operation
- Supports Toggle Mode flash
- Supports ONFI 1.X/ONFI 2.X/ONFI 3.X NAND Flash

- Low power consumption
- Enhanced ESD design
- Non-Direct remap architecture
- Manufacturing utility ready

4.2. AK2705EN Function Block Diagram

The following diagram is the internal block diagram of AK2705EN.

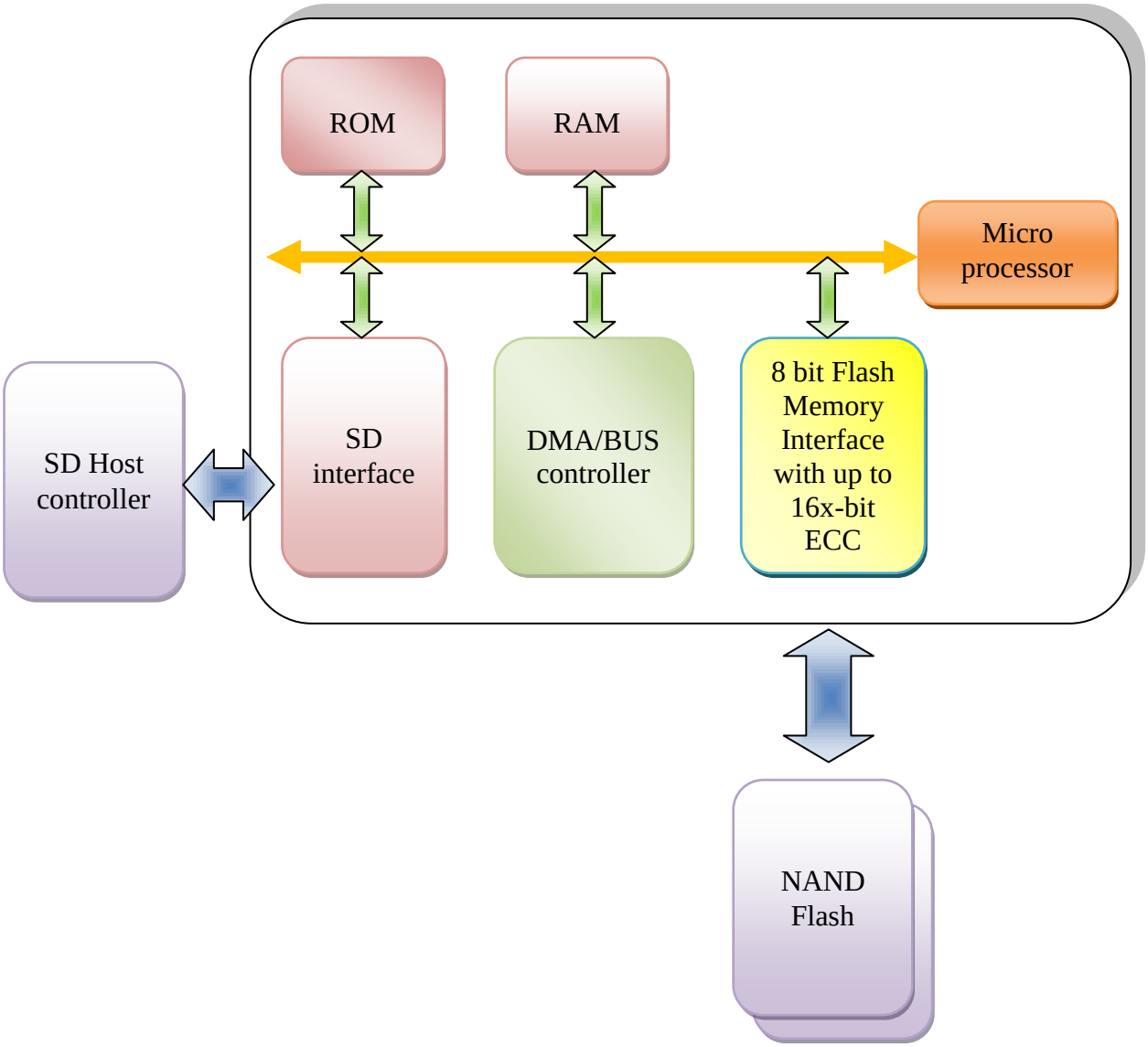

Figure 4-1 AK2705EN Function Block Diagram

5. Pin Description

5.1. Flash Interface

Pin Name	Direction	Description
DATA_FM [7:0]	I/O	Flash interface data bus, direct connect to the flash memory
CLE_FM	O	Flash interface command latch enable, direct connect to the flash memory
ALE_FM	O	Flash interface address latch enable, direct connect to the flash memory
RD_FM_N	O	Flash interface read strobe control, direct connect to the flash memory
WR_FM_N	O	Flash interface write strobe control, direct connect to the flash memory
WP_FM_N	O	Flash interface write protection, direct connect to the flash memory
READY_FM [0]	I	Used as busy signal from flash memory
CE_FM_N [0]	O	Used as flash chip select signal. Max. 1 flash chips can connect to AK2705EN

Table 5-1 Flash Interface

5.2. SD Interface

Pin Name	Direction	Description
CMD_SD	I/O	SD interface command line
DATA_SD [3:0]	I/O	SD interface data line
CLK_SD	I	SD interface synchronous clock input

Table 5-2 SD Interface

5.3. Other Function Pin

Pin Name	Direction	Description
DNU	-	Do not use

Table 5-3 Other Function Pin

5.4. Voltage Regulator

Pin Name	Direction	Description
VCC	Power in	Regulator in. Direct connect to card source power
GNDA	Ground	Analog ground
VCORE	Power out	Regulator 1.2V output for always-on core power supply
VCCK	Power out	Regulator 1.2V output for core power supply
V25	Power out	Regulator 2.5V output for flash core
VCCIOF	Power out	Regulator 1.2V or 1.8V output for flash interface IO
VCCIOM	Power out	Regulator 1.8V or VCC output for SD interface IO

Table 5-4 Voltage Regulator

5.5. Other Power Pin

Pin Name	Direction	Description
VCCK	Power in	1.2V power supply for core power
VCORE	Power in	1.2V power supply for always-on core power
VSSK	Ground	Core ground
VCC3IOF	Power in	1.2V/1.8V power supply for flash interface IO
VSSIOF	Ground	Flash IO pad ground
VCC3IOM	Power in	Power supply for SD interface IO
VSS3IOM	Ground	SD IO pad ground

Table 5-5 Other Power Pin

6. Package Description

6.1. Physical Pin Assignment Data Chip On Board

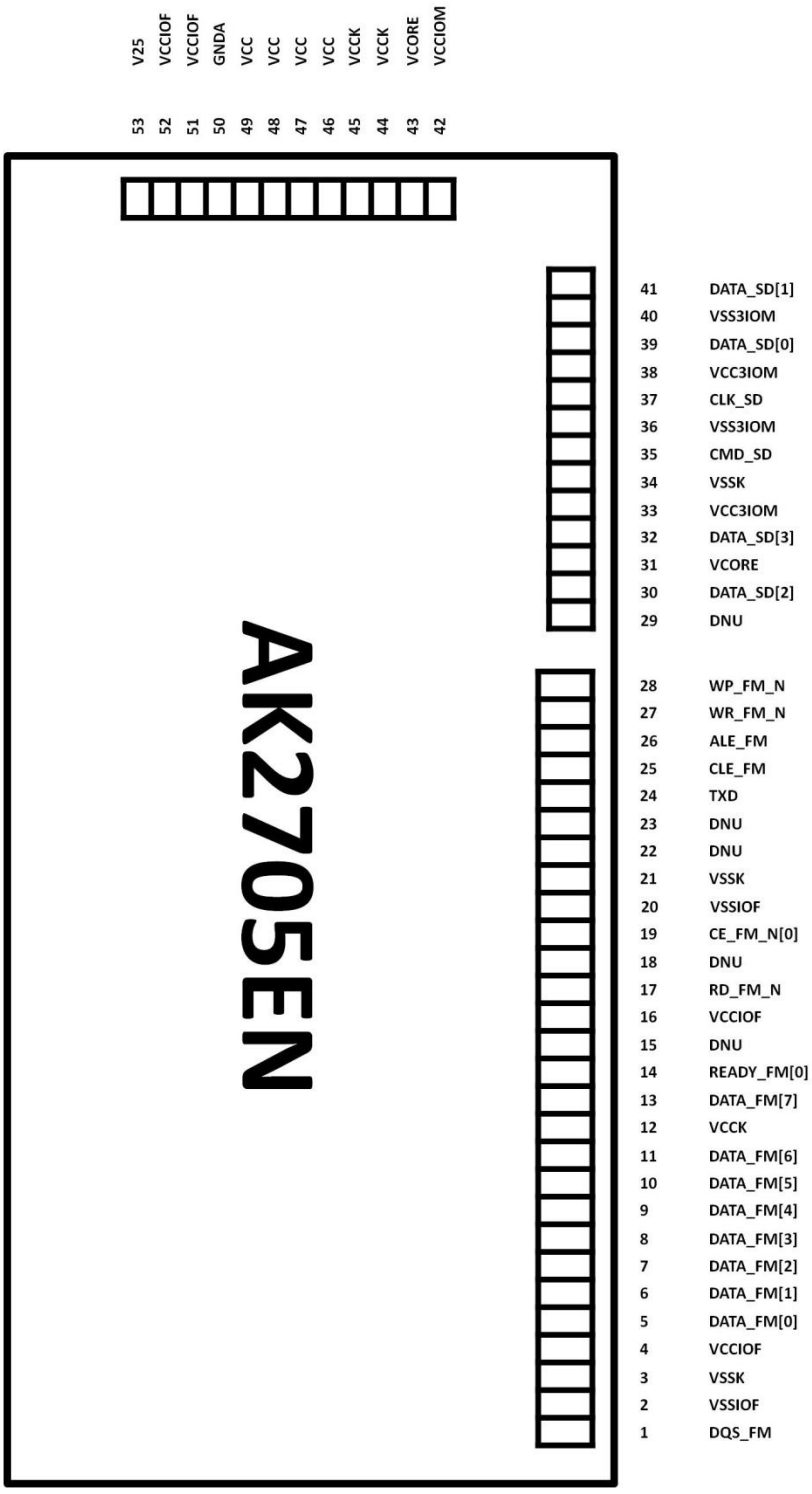

Figure 6-1 AK2705EN pin diagram (Top view, die)

6.2. Die Information

Die size with scribe line is, 2330.00um x 1214.00um (Scribe Line : 62um):

- Lower left (0,0)
- Upper right: (2330.00, 1214.00)

Die size without scribe line is, 2268.00um x1152.00um

Table 6-1 shows pad XY coordinate of SD Memory Card Controller.

Pad No.	Text	X Pad Open	Y Pad Open	X Pad Bond	Y Pad Bond
1	DQS_FM	48.60	72.62	2214.00	1113.87
2	VSSIOF	48.60	72.62	2160.00	1113.87
3	VSSK	48.60	72.62	2106.00	1113.87
4	VCCIOF	48.60	72.62	2052.00	1113.87
5	DATA_FM[0]	48.60	72.62	1998.00	1113.87
6	DATA_FM[1]	48.60	72.62	1944.00	1113.87
7	DATA_FM[2]	48.60	72.62	1890.00	1113.87
8	DATA_FM[3]	48.60	72.62	1836.00	1113.87
9	DATA_FM[4]	48.60	72.62	1782.00	1113.87
10	DATA_FM[5]	48.60	72.62	1728.00	1113.87
11	DATA_FM[6]	48.60	72.62	1674.00	1113.87
12	VCCK	48.60	72.62	1620.00	1113.87
13	DATA_FM[7]	48.60	72.62	1566.00	1113.87
14	READY_FM[0]	48.60	72.62	1512.00	1113.87
15	DNU	48.60	72.62	1458.00	1113.87
16	VCCIOF	48.60	72.62	1404.00	1113.87
17	RD_FM_N	48.60	72.62	1350.00	1113.87
18	DNU	48.60	72.62	1296.00	1113.87
19	CE_FM_N[0]	48.60	72.62	1242.00	1113.87
20	VSSIOF	48.60	72.62	1188.00	1113.87
21	VSSK	48.60	72.62	1134.00	1113.87
22	DNU	48.60	72.62	1080.00	1113.87
23	DNU	48.60	72.62	1026.00	1113.87
24	TXD	39.60	72.62	976.50	1113.87
25	CLE_FM	48.60	72.62	927.00	1113.87
26	ALE_FM	48.60	72.62	873.00	1113.87
27	WR_FM_N	48.60	72.62	819.00	1113.87
28	WP_FM_N	48.60	72.62	765.00	1113.87
29	DNU	39.60	72.62	697.50	1113.87
30	DATA_SD[2]	48.60	72.62	648.00	1113.87
31	VCORE	48.60	72.62	594.00	1113.87
32	DATA_SD[3]	48.60	72.62	540.00	1113.87
33	VCC3IOM	48.60	72.62	486.00	1113.87

Pad No.	Text	X Pad Open	Y Pad Open	X Pad Bond	Y Pad Bond
34	VSSK	48.60	72.62	432.00	1113.87
35	CMD_SD	48.60	72.62	378.00	1113.87
36	VSS3IOM	48.60	72.62	324.00	1113.87
37	CLK_SD	48.60	72.62	270.00	1113.87
38	VCC3IOM	48.60	72.62	216.00	1113.87
39	DATA_SD[0]	48.60	72.62	162.00	1113.87
40	VSS3IOM	48.60	72.62	108.00	1113.87
41	DATA_SD[1]	48.60	72.62	54.00	1113.87
42	VCCIOM	72.62	48.60	38.13	647.11
43	VCORE	72.62	48.60	38.13	593.11
44	VCCK	72.62	48.60	38.13	539.11
45	VCCK	72.62	48.60	38.13	485.11
46	VCC	72.62	48.60	38.13	431.11
47	VCC	72.62	48.60	38.13	377.11
48	VCC	72.62	48.60	38.13	323.11
49	VCC	72.62	48.60	38.13	269.11
50	GNDA	72.62	48.60	38.13	215.11
51	VCCIOF	72.62	48.60	38.13	161.11
52	VCCIOF	72.62	48.60	38.13	107.11
53	V25	72.62	48.60	38.13	53.11

Table 6-1 Pad XY Coordination

7. Electrical Characteristics

The SD Memory Card Controller is used to provide an interface between on-chip bus and external (off-chip) memory devices.

7.1. General DC Character

Parameter	Symbol	Min.	Max.	Unit	Remark
Peak voltage on all lines	-	-0.3	3.6	V	
All input leakage current	-	-10	10	uA	
All output leakage current	-	-10	10	uA	
Supply voltage for low voltage range	V_{DDL}	-	-	V	
Supply voltage for high voltage range	V_{DDH}	2.7	3.6	V	
Supply voltage differential	-	-0.5	0.5	V	

Table 7-1 General DC Character

7.2. Bus Signal Line Loading

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull up resistance for SD command line	R_{CMD}	4.7	100	Kohm	
Pull up resistance for SD data line	R_{DAT}	10	100	Kohm	
Total Bus capacitance for each signal line	C_L	-	30	pF	
Signal line inductance	-	-	16	pF	
Pull-up resistance inside card (pin 1)	R_{DAT3}	10	150	Kohm	

Table7-2 Bus Signal Line Loading

7.3. Bus Signal Level

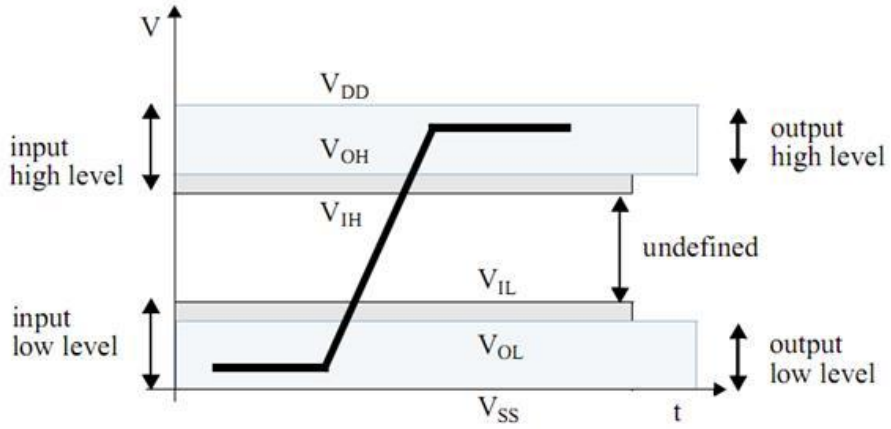

Figure 7-1 Bus Signal Level

Parameter	Symbol	Min.	Max.	Unit	Remark
Output High voltage	V_{OH}	2.4	-	V	V_{DD} = 3.3V
Output Low voltage	V_{OL}	-	0.4	V	V_{DD} = 3.3V
Input High voltage	V_{IH}	2.0	3.6	V	V_{DD} = 3.3V
Input Low voltage	V_{IL}	-0.3	0.8	V	V_{DD} = 3.3V
Output High voltage	V_{OH}	1.4	-	V	V_{DD} = 1.8V
Output Low voltage	V_{OL}	-	0.45	V	V_{DD} = 1.8V
Input High voltage	V_{IH}	1.26	2.1	V	V_{DD} = 1.8V
Input Low voltage	V_{IL}	-0.3	0.58	V	V_{DD} = 1.8V

Table 7-3 Bus Signal Level

7.4. Bus Timing for SD Card in Default Mode

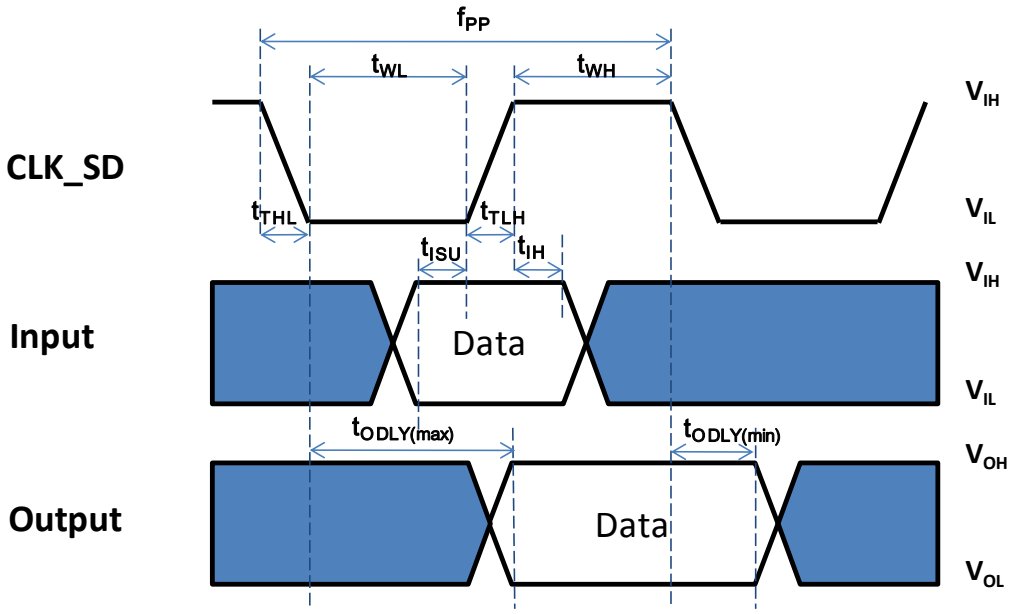

Figure 7-2 Timing diagram data input/output referenced to clock (SD card in default speed mode)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK_SD					
Clock frequency data transfer mode	f_{PP}	-	25	MHz	C_L ≦ 10pF (1 card)
Clock frequency identification mode	f_{OD}	-	400	KHz	C_L ≦ 10pF (1 card)
Clock low time / Clock high time	t_{WL}/t_{WH}	10	-	ns	C_L ≦ 10pF (1 card)
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	10	ns	C_L ≦ 10pF (1 card)
Input CMD_SD/DATA_SD, reference to CLK_SD					
Input set-up time	t_{ISU}	5	-	ns	C_L ≦ 10pF (1 card)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input hold time	t_{IH}	5	-	ns	$C_L \leqq$ 10pF (1 card)
Output CMD_SD/DATA_SD, reference to CLK_SD					
Output delay time during Data Transfer Mode	t_{ODLY}	-	14	ns	CL $\leqq$ 40pF (1 card)
Output delay time during Identification Mode	t_{ODLY}	-	50	ns	CL $\leqq$ 40pF (1 card)

Table 7-4 Default speed mode timing for SD card (low speed)

(1) All timing values are measured relative to 50% of voltage level.

(2) Clock Rise and fall times are measured from VIH to VIL of voltage level.

7.5. Bus Timing for SD Card in High-Speed Mode

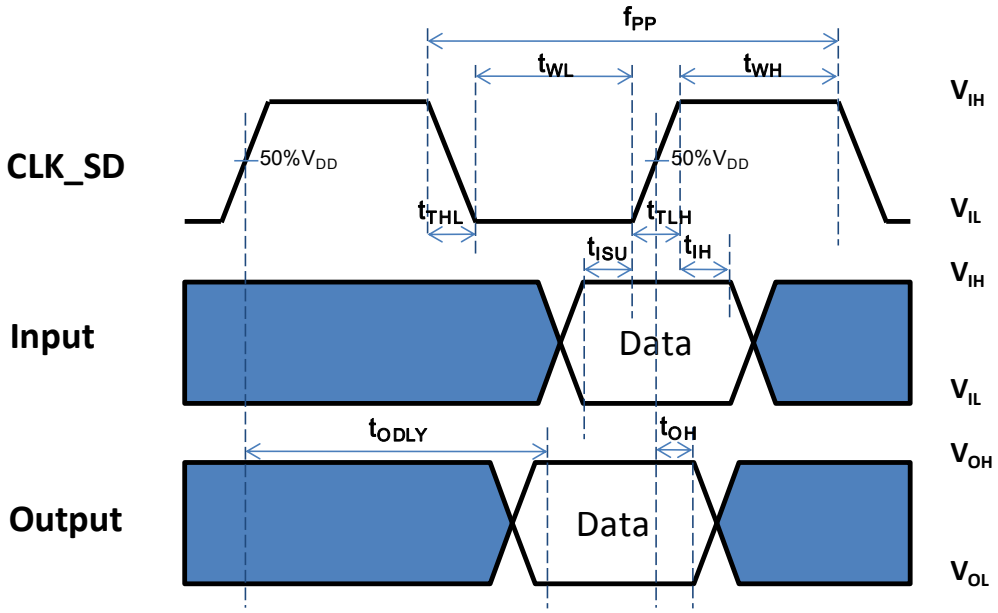

Figure 7-3 Timing diagram data input/output referenced to clock (SD card in high speed mode)

7.5.1. High Speed Mode Timing for SD Card

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK_SD					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	$C_L \leqq$ 10pF (1 card)
Clock low time / Clock high time	t_{WL}/t_{WH}	7	-	ns	$C_L \leqq$ 10pF (1 card)
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	3	ns	$C_L \leqq$ 10pF (1 card)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CMD_SD/DATA_SD, reference to CLK_SD					
Input set-up time	t_{ISU}	6	-	ns	$C_L \leqq$ 25pF (1 card)
Input hold time	t_{IH}	2	-	ns	$C_L \leqq$ 25pF (1 card)
Output CMD_SD/DATA_SD, reference to CLK_SD					
Output delay time during data transfer mode	t_{ODLY}		14	ns	$C_L \leqq$ 40pF (1 card)
Output hold time	t_{OH}	2.5		ns	$C_L \geqq$ 15pF (1 card)
Total System capacitance for each line	C_L		40	pF	

Table 7-5 High speed mode timing for SD card

(1) All timing values are measured relative to 50% of voltage level.

(2) Rise and fall times are measured from 10% - 90% of voltage level

7.5.2. SDR104/SDR50/SDR25/SDR12 Mode Timing for SD Card

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK_SD					
Clock frequency data transfer mode	f_{PP}	0	208	MHz	C_L = 10pF
Clock cycle time	t_{CLK}	4.8	-	ns	C_L = 10pF
Clock duty cycle		30	70	%	
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	$0.2*t_{CLK}$	ns	C_L = 10pF
Input CMD_SD/DATA_SD, reference to CLK_SD					
Input set-up time for SDR104	t_{ISU}	1.4	-	ns	C_L = 10pF
Input set-up time for SDR50	t_{ISU}	3	-	ns	C_L = 10pF
Input hold time	t_{IH}	0.8	-	ns	C_L = 5pF
Output CMD_SD/DATA_SD, reference to CLK_SD					
Output delay time for SDR50	t_{ODLY}	-	7.5	ns	C_L = 30 pF, using driver Type B
Output delay time for SDR25 and SDR12	t_{ODLY}		14	ns	C_L = 40 pF, using driver Type B
Output hold time	t_{OH}	1.5		ns	C_L = 15pF
Total System capacitance for each line	C_L		40	pF	

Table 7-6 SD50/SDR25/SDR12 mode timing for SD card

7.6. Bus Timing for SD Card in DDR Mode

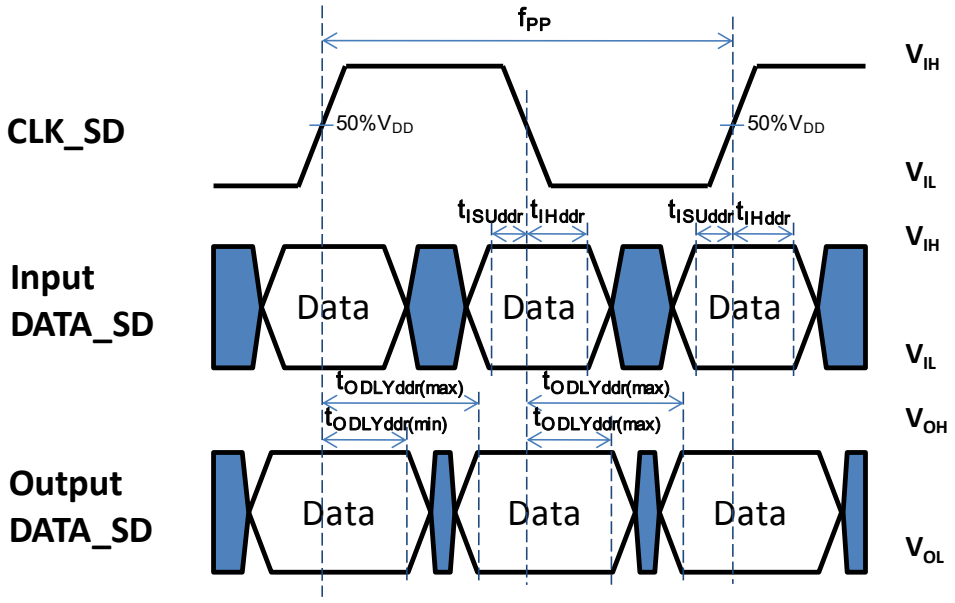

Figure 7-4 Timing diagram data input/output referenced to clock (DDR mode)

7.6.1. DDR Mode Timing for SD Card

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK_SD					
Clock duty cycle		45	55	%	
Input CMD_SD, reference to CLK_SD					
Input set-up time	t_{ISU}	3	-	ns	$C_L \leqq$ 10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_L \leqq$ 10pF (1 card)
Output CMD_SD, reference to CLK_SD					
Output delay time during data transfer mode	t_{ODLY}	-	13.7	ns	$C_L \leqq$ 30pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	$C_L \geqq$ 15pF (1 card)
Input DATA_SD, reference to CLK_SD					
Input set-up time	t_{ISUddr}	3	-	ns	$C_L \leqq$ 10pF (1 card)
Input hold time	t_{IHddr}	0.8	-	ns	$C_L \leqq$ 10pF (1 card)
Output DATA_SD, reference to CLK_SD					
Output delay time during data transfer mode	$t_{ODLYddr}$	-	7	ns	$C_L \leqq$ 25pF (1 card)
Output hold time	$t_{ODLYddr}$	1.5	-	ns	$C_L \geqq$ 15pF (1 card)

Table 7-7 DDR mode timing for SD card

7.7. Flash Interface AC Characteristic

Parameter	Symbol	Min.	Max.	Unit	Remark
CLE SETUP TIME	t_{CLS}	27.5	-	ns	
CLE Hold Time	t_{CLH}	12.5	-	ns	
ALE Setup Time	t_{ALS}	25	-	ns	
ALE Hold Time	t_{ALH}	10	-	ns	
WE Pulse Width	t_{WP}	15	-	ns	
Data Setup Time	t_{DS}	25	-	ns	
Data Hold Time	t_{DH}	12.5	-	ns	
Write Cycle Time	t_{WC}	37.5	-	ns	
WE High Hold Time	t_{WH}	20	-	ns	
Read Cycle Time	t_{RC}	37.5	-	ns	
RE pulse Width	t_{RP}	17.5	-	ns	
RE High Hold Time	t_{REH}	20	-	ns	

Table 7-8 Flash Interface AC Characteristic

7.7.1. Command Latch Cycle

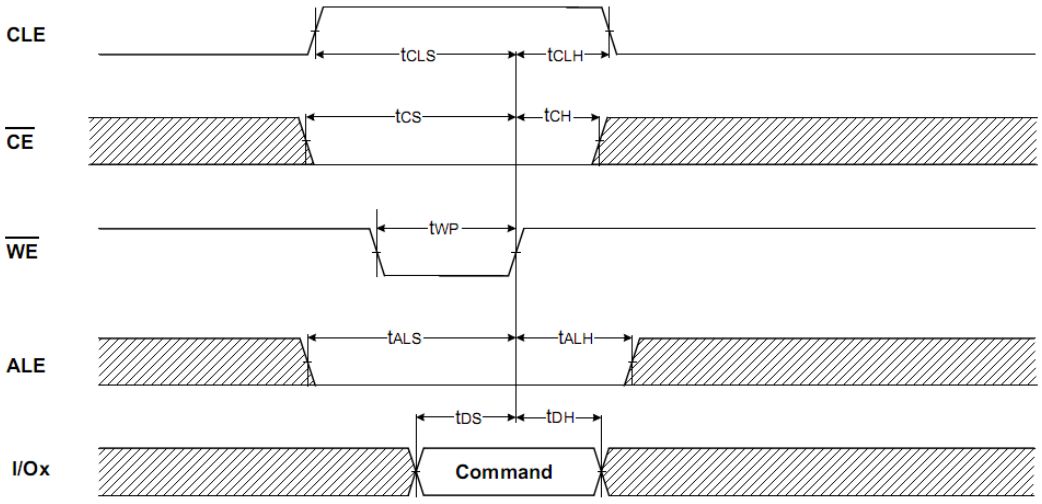

Figure 7-5 Command Latch Cycle

7.7.2. Address Latch Cycle

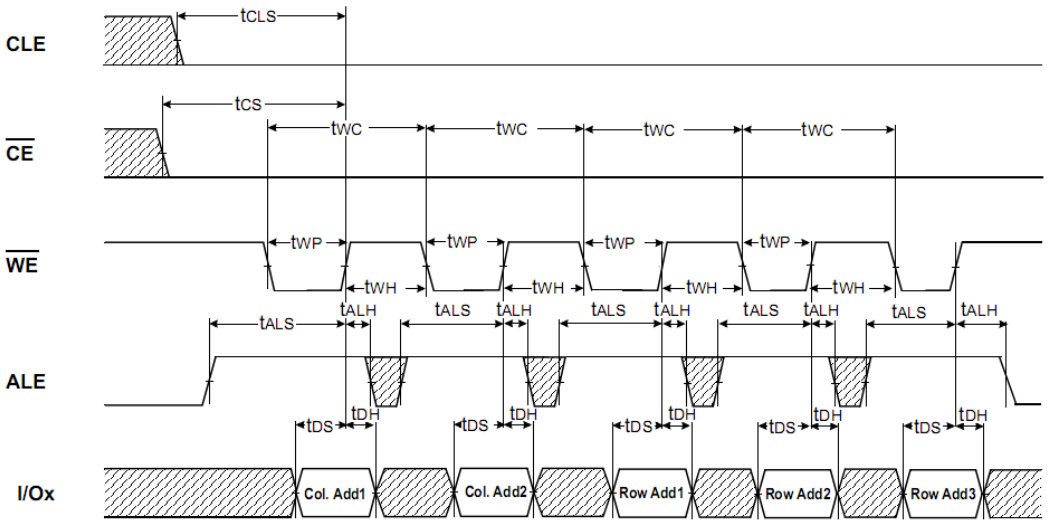

Figure 7-6 Address Latch Cycle

7.7.3. Input Data Latch Cycle

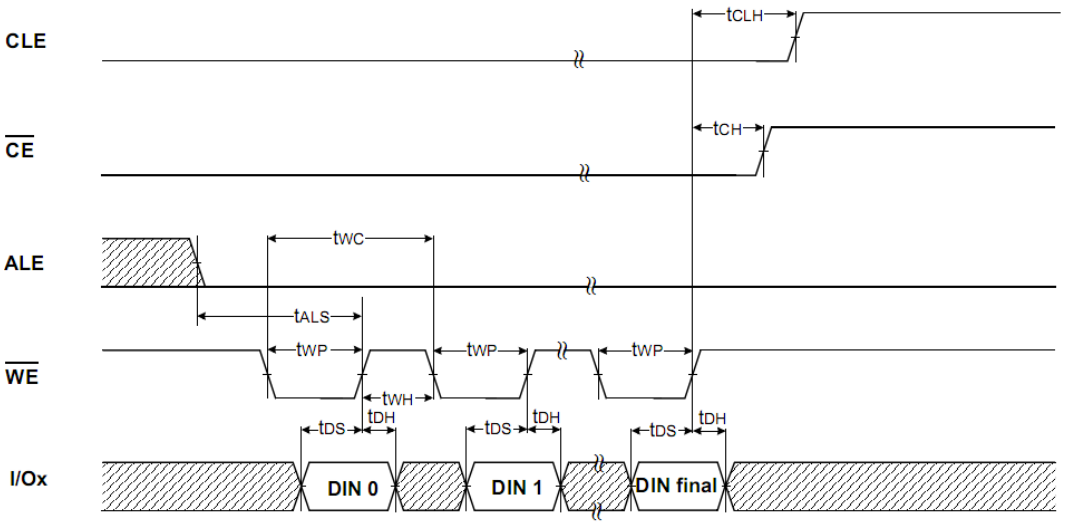

Figure 7-7 Input Data Latch Cycle

7.7.4. Sequential Out Cycle after Read (CLE=L,/WE=H,ALE=L)

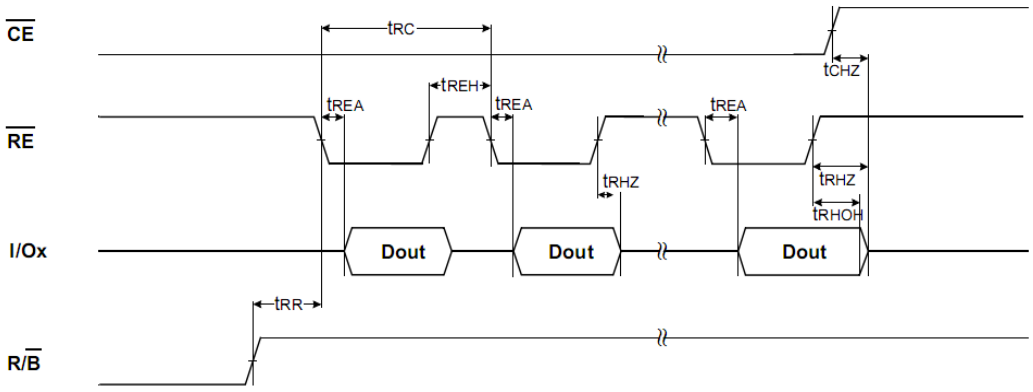

Figure 7-8 Sequential Out Cycle after Read (CLE=L,/WE=H,ALE=L)

7.8. Power Consumption (Reserved)

Parameter	Symbol	Typ.	Max.	Unit	Remark
Read current at 3.3V		30	40	mA	VDD = 3.3V
Write current at 3.3V		30	40	mA	VDD = 3.3V
Pre-initialization standby current at 3.3V		40	50	uA	VDD = 3.3V
Post-initialization standby current at 3.3V		40	50	uA	VDD = 3.3V

Table 7-9 power Consumption

8. SD Register Description

The design parameters are parameters that control the implementation of RTL design by Verilog parameter or VHDL generic. The purpose of parameter is to make the hardware design reusable on different conditions.

Software designer should refer to the particular implementation to do the programming. This section introduces the register in SD and the values that AK2705EN used. The following table is the register list of current specification. The detail functionality is not described here; please reference to latest SD specifications.

Register Name	SD 6.1	SD 6.0	SD 5.1	SD 4.1	SD 3.01	SD 2.02	SD 1.1	SD 1.01
Operation Condition Register (OCR)	V	V	V	V	V	V	V	V
Card Identification Register (CID)	V	V	V	V	V	V	V	V
Driver Stage Register (DSR)	V	V	V	V	V	V	V	V
Relative Card Address Register (RCA)	V	V	V	V	V	V	V	V
Card Specific Data Register (CSD)	V	V	V	V	V	V	V	V
SD card Configuration Register (SCR)	V	V	V	V	V	V	V	V

Table 8-1 SD Register table

8.1. SD Operation Condition Register (OCR)

The 32-bit operation conditions register stores the VDD voltage profile of the card. In addition, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit. The OCR register shall be implemented by all cards. The supported voltage range is coded as shown in the following table, for High Voltage and Dual voltage SD. As long as the card is busy, the corresponding bit (31) is set to LOW. Bit 7 of OCR is newly defined for Dual Voltage Card and set to 0 in default. If a Dual Voltage Card does not receive CMD8, OCR bit 7 in the response indicates 0, and the Dual Voltage Card which received CMD8, sets the bit to 1.

Additionally, this register includes 2 more status information bits. Bit 31 – Card power up status bit, this status bit is set if the card power up procedure has been finished. Bit 30 – Card capacity status bit, this status bit is set to 1 if card is High Capacity SD Memory Card. 0 indicates that the card is Standard Capacity SD Memory Card. The Card Capacity status bit is valid after the card power up procedure is completed and the card power up status bit is set to 1. The Host shall read this status bit to identify a Standard or High Capacity SD Memory Card.

OCR bit	VDD voltage window	High voltage SD	Dual voltage SD
[6:0]	Reserved	000 0000 b	000 0000 b
[7]	1.7V~1.95V	0 b	1 b
[14:8]	2.0V – 2.6V	000 0000 b	000 0000 b
[23:15]	2.7V – 3.6V	1 1111 1111 b	1 1111 1111 b
[24]	Switch to 1.8V Accepted		
[29:25]	Reserved	00 0000 b	00 0000 b
[30]	Card capacity status		
[31]	Card power up status bit		

Table 8-2 SD OCR Table

(1) Pin “LVMOD” should connect to low for high voltage SD, and connect to high for dual voltage SD.

(2) OCR bit [31] is set to LOW if the card has not finished the power up routine.

(3) OCR bit [30] is valid only when the card power up status bit is set.

(4) Only UHS-I card can support the OCR bit [24].

8.2. SD Card Identification Register (CID)

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following table.

CID bit	width	Name	Field
[127:120]	8	Manufacture ID	MID
[119:104]	16	OEM/Application ID	OID
[103:64]	40	Product Name	PNM
[63:56]	8	Product Revision	PRV
[55:24]	32	Product Serial Number	PSN
[23:20]	4	Reserved	-
[19:8]	12	Manufacturing Date	MDT
[7:1]	7	CRC7 check sum	CRC
[0]	1	Not used, always ‘1’	-

Table 8-3 SD CID Table

(1) All content in the CID table is programmable. Manufacturer can update the CID data through ASolid utility.

(2) Manufacturer should license MID & OID field from SDA.

8.3. SD Driver Stage Register (DSR)

The 16-bit driver stage register is optionally used to improve the bus performance for extended operating conditions. The CSD register carries the information about the DSR register usage.

8.4. SD Relative Card Address Register (RCA)

The writable 16-bit relative card address register carries the card address this is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

8.5. SD Card Specific Data Register (CSD)

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time and data transfer speed, whether the DSR register can be used etc. The programmable part of the register can be changed by CMD27.

8.5.1. CSD Version 2.0

CSD bit	Width	Name	Field	Value	Note
[127:126]	2	CSD structure	CSD_STRUCTURE	01b	v2.0 (High Capacity and Extended Capacity)
[125:120]	6	Reserved	-	-	-
[119:112]	8	Data read access-time 1	TAAC	0Eh	1 ms (*3)
[111:104]	8	Data read access-time 2	NSAC	00h	(*3)
[103:96]	8	Max. data transfer rate	TRAN_SPEED	32h	25 MHz
[95:84]	12	Card command classes	CCC	5F5h	(*1)
[83:80]	4	Max. read data block length	READ_BL_LEN	9h	512 bytes(*3)
[79]	1	Partial block read allowed	READ_BL_PARTIAL	0b	Not Support(*3)
[78]	1	Write block misalignment	WRITE_BLK_MISALIGN	0b	Not Support(*3)

CSD bit	Width	Name	Field	Value	Note
[77]	1	Read block misalignment	READ_BLK_MISALIGN	0b	Not Support(*3)
[76]	1	DSR implemented	DSR_IMP	0b	Not support
[75:70]	6	Reserved	-	00h	-
[69:48]	22	Device size	C_SIZE	(*2)	(*2)
[47]	1	Reserved	-	0	-
[46]	1	Erase single block enable	ERASE_BLK_EN	1b	allowed(*3)
[45:39]	7	Erase sector size	SECTOR_SIZE	7Fh	64KB(*3)
[38:32]	7	Write protect group size	WP_GRP_SIZE	00h	(*3)
[31]	1	Write protect group enable	WP_GRP_ENABLE	0b	Not Support(*3)
[30:29]	2	Reserved	-	-	-
[28:26]	3	Write speed factor	R2W_FACTOR	010b	4X(*3)
[25:22]	4	Max. write data block length	WRITE_BL_LEN	9h	512 bytes(*3)
[21]	1	Partial block write allowed	WRITE_BL_PARTIAL	0b	Not Support(*3)
[20:16]	5	Reserved	-	-	-
[15]	1	File format group	FILE_FORMAT_GRP	0b	HD like FAT(*3)
[14]	1	Copy flag	COPY	0b	Not copied
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	0 b	Not protected
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	0 b	Not protected
[11:10]	2	File format	FILE_FORMAT	00 b	HD like FAT(*3)
[9:8]	2	ECC code	ECC	00 b	None
[7:1]	7	CRC	CRC	-	-
[0]	1	Not used, always ‘1’	-	1 b	-

Table 8-4 CSD Version 2.0 Table

(*1) Support command class 0, 2, 4, 5, 6, 7, 8 and10. Include: Basic, Block read/write, Erase, Write protection, application command, Lock card and switch function. Not support 1 and 3. Include: Stream read/write.

(*2) ~ (*4) This field is not a constant value. The value will be changed by different flash memory. For example, the value of Samsung SLC flash is different from Toshiba MLC flash.

(*3) The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enable host, which refers to these fields, to keep

compatibility to CSD Version 1.0.

Note: bit [15:0] is programmable by host side. Please reference to SD specification for detail information.

8.5.2. CSD Version 1.0

CSD bit	Width	Name	Field	Value	Note
[127:126]	2	CSD structure	CSD_STRUCTURE	00 b	v1.0 (standard capacity)
[125:120]	6	Reserved	-	-	-
[119:112]	8	Data read access-time 1	TAAC	7F h	80 ms
[111:104]	8	Data read access-time 2	NSAC	FF h	25.5k clocks
[103:96]	8	Max. data transfer rate	TRAN_SPEED	32 h	25 MHz
[95:84]	12	Card command classes	CCC	5F5 h	(*1)
[83:80]	4	Max. read data block length	READ_BL_LEN	9 h	512 bytes
[79]	1	Partial block read allowed	READ_BL_PARTIAL	1 b	Support
[78]	1	Write block misalignment	WRITE_BLK_MISALIGN	1 b	Support
[77]	1	Read block misalignment	READ_BLK_MISALIGN	1 b	Support
[76]	1	DSR implemented	DSR_IMP	0 b	Not support
[75:74]	2	Reserved	-	-	
[73:62]	12	Device size	C_SIZE	(*2)	(*2)
[61:59]	3	Min. read current @ VDD	VDD_R_CURR_MIN	101 b	35 mA
[58:56]	3	Max read current @ VDD	VDD_R_CURR_MAX	101 b	45 mA
[55:53]	3	Min write current @ VDD	VDD_W_CURR_MIN	101 b	35 mA
[52:50]	3	Max write current @ VDD	VDD_W_CURR_MAX	101 b	45 mA
[49:47]	3	Device size multiplier	C_SIZE_MULT	(*2)	(*2)
[46]	1	Erase single block enable	ERASE_BLK_EN	0 b	Not allowed
[45:39]	7	Erase sector size	SECTOR_SIZE	(*3)	(*3)
[38:32]	7	Write protect group size	WP_GRP_SIZE	(*4)	(*4)
[31]	1	Write protect group enable	WP_GRP_ENABLE	1 b	Support
[30:29]	2	Reserved	-	-	-
[28:26]	3	Write speed factor	R2W_FACTOR	101 b	32X
[25:22]	4	Max. write data block length	WRITE_BL_LEN	9 h	512 bytes
[21]	1	Partial block write allowed	WRITE_BL_PARTIAL	1 b	Support
[20:16]	5	Reserved	-	-	-
[15]	1	File format group	FILE_FORMAT_GRP	0 b	HD like FAT
[14]	1	Copy flag	COPY	0 b	Not copied
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	0 b	Not protected

CSD bit	Width	Name	Field	Value	Note
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	0 b	Not protected
[11:10]	2	File format	FILE_FORMAT	00 b	HD like FAT
[9:8]	2	ECC code	ECC	00 b	None
[7:1]	7	CRC	CRC	-	-
[0]	1	Not used, always '1'	-	1 b	-

Table 8-5 CSD Version 1.0 Table

(*1) Support command class 0, 2, 4, 5, 6, 7, 8 and 10. Include: Basic, Block read/write, Erase, Write protection, application command, Lock card and switch function. Not support 1 and 3. Include: Stream read/write.

(*2) ~ (*4) This field is not a constant value. The value will be changed by different flash memory. For example, the value of Samsung SLC flash is different from Toshiba MLC flash.

Note: bit [15:0] is programmable by host side. Please reference to SD specification for detail information.

8.6. SD card Configuration Register (SCR)

The CSD register is another configuration register in SD card. SCR provides on SD card's special features that were configured into the given card. The size of SCR is 64 bit. SCR is a read only register.

SCR bit	Width	Name	Field	Value	Note
[63:60]	4	SCR structure	SCR_STRUCTURE	0000 b	v1.0-v3.01
[59:56]	4	SD card spec. version	SD_SPEC	0010 b	V1.10 or V2.0 or higher
[55]	1	Data status after erase	DATA_STAT_AFTER_ERASE	0 b	Zero after erase
[54:52]	3	CPRM Security Specification Version	SD_SECURITY	010 b	SDSC Card
				011 b	SDHC Card
				100 b	SDXC Card
[51:48]	4	DAT bus width support	SD_BUS_WIDTH	0101 b	Support 1/4 bit
[47]	1	Spec. Version 3.00 or higher	SD_SPEC3	1 b	V3.0X or higher
[46:43]	4	Extended Security Support	EX_SECURITY	0000 b	Support extended security
[42]	1	Spec. Version 4.00 or higher	SD_SPEC4	1 b	V4.XX or higher

SCR bit	Width	Name	Field	Value	Note
[41:38]	4	Spec. Version 5.00 or higher	SD_SPECX	0010 b	V5.XX or higher
[37:36]	2	Reserved	-		
[35:32]	4	Command Support bits	CMD58/59_SUPPORT	1 b	Optional. If CMD58/59 is supported, CMD48/49 shall be supported
			CMD48/49_SUPPORT	1 b	Optional
			CMD23_SUPPORT	1 b	SDR[33], mandatory for UHS104 card
			CMD20_SUPPORT	1 b	SDR[32], mandatory for SDXC card
[31:0]	32	Reserved	-	-	-

Table 8-6 SD SCR Table

9. Application

The following figure is the typical application block diagram of AK2705EN.

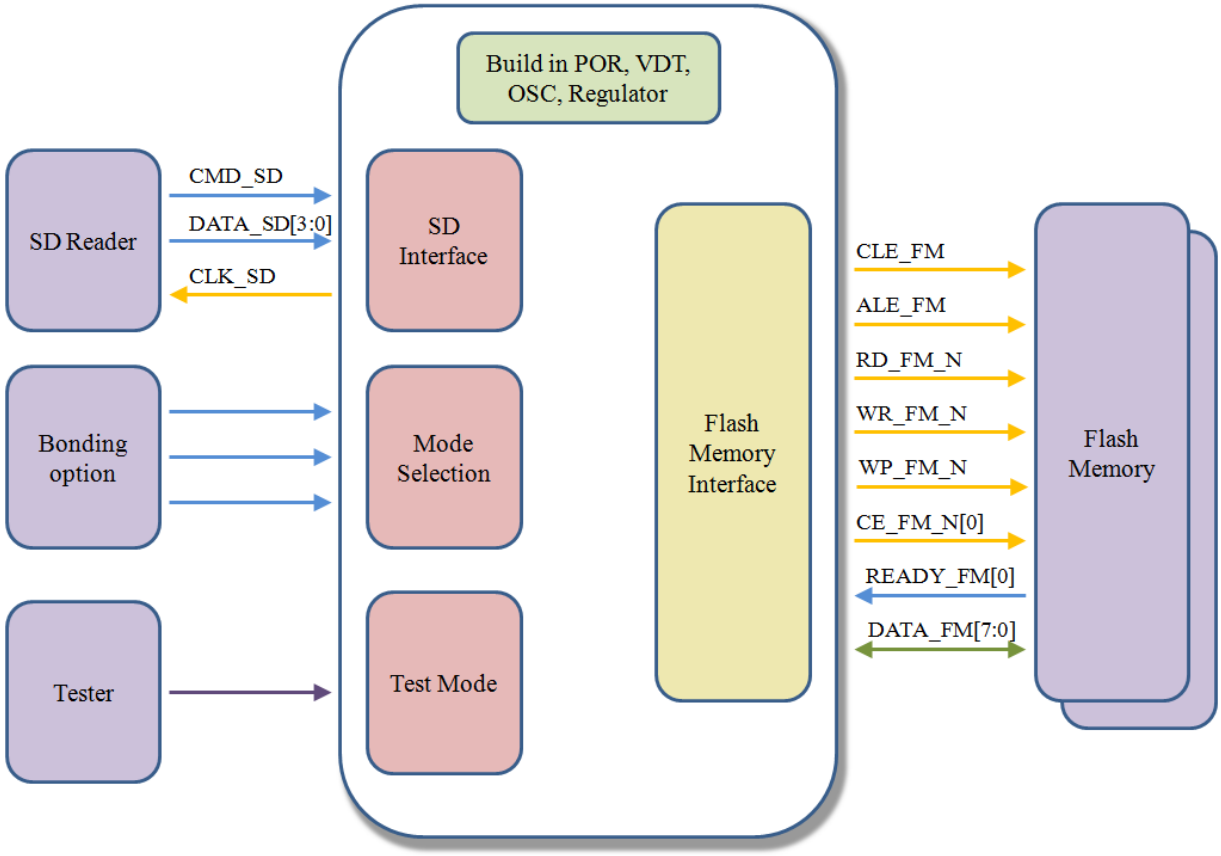

Figure 9-1 AK2705EN application block diagram